DYNAMIC SOLUTIONS

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74LS107N Dual JK Negative Edge Triggered Flip-Flop IC

Features:

The 74LS107N is a dual JK flip-flop with negative edge triggering and independent J, K, clock, and direct clear inputs. The device changes output state on the high to low transition of the clock signal, while a low level on the clear input forces the output low regardless of other inputs. Designed with TTL technology, it offers fast switching, stable performance, and is suitable for counters, frequency division, and sequential logic circuits.

Specifications	
Supply Voltage (VCC)	4.75V to 5.25V
Input HIGH Voltage (VIH)	2.0V min
Input LOW Voltage (VIL)	0.8V max
Output HIGH Voltage (VOH)	2.7V min
Output LOW Voltage (VOL)	0.5V max
Output Current High (IOH)	-0.4 mA
Output Current Low (IOL)	8 mA
Max Clock Frequency	45 MHz
Propagation Delay	15 to 20 ns
Operating Temperature	0C to 70C
Usage	Counters, frequency division, sequential logic

Pinouts:

Pin Name	Type	Description
J1	Input	J input flip-flop 1
Q1	Output	Output flip-flop 1
Q1	Output	Complement output flip-flop 1
K1	Input	K input flip-flop 1
Q2	Output	Output flip-flop 2
Q2	Output	Complement output flip-flop 2
GND	Power	Ground
J2	Input	J input flip-flop 2
CP2	Input	Clock input flip-flop 2
CD2	Input	Clear input flip-flop 2
K2	Input	K input flip-flop 2
CP1	Input	Clock input flip-flop 1
CD1	Input	Clear input flip-flop 1
VCC	Power	Supply voltage

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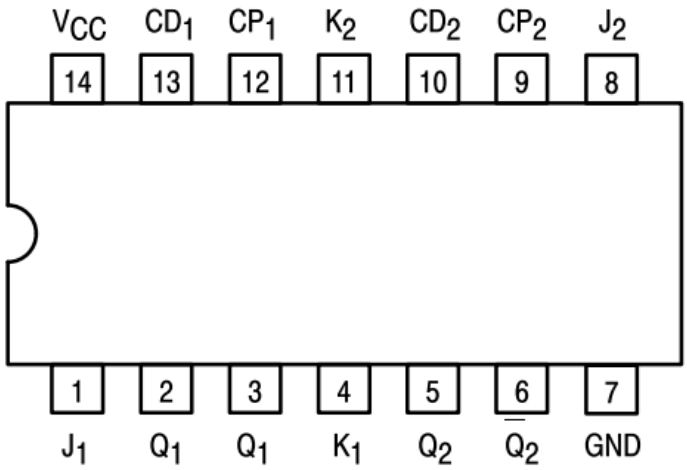

Product Pictures: